What's New in Quartus II Software Version 2.2

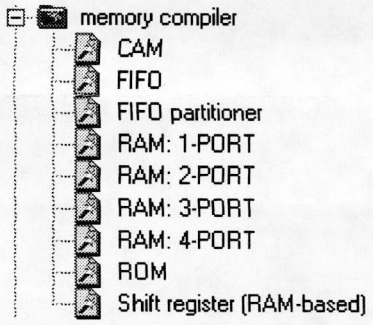
The Quartus® II software version 2.2 simplifies SOPC design by including a redesigned and more intuitive user interface design, a new interface to create and configure memory, push-button performance enhancements, and new incremental routing features in the SignalTap® II Embedded Logic Analyzer to shorten verification cycles.

Additionally, version 2.2 of the Quartus II software features enhancements and improvements in design, synthesis, LogicLock™ block-based design flow, fitting, verification, and device support.

Design

- Redesigned user interface
  - Removal of modes; compile, simulate, and software build menu commands are available at all times
  - New Assignment menu provides access to all device, pin, and other assignment options as well as access to all settings windows and floorplan editors
  - New **Settings** dialog box (Assignments menu) includes all settings options
  - New Assignment Editor provides spreadsheet like interface to view and make assignments (Assignment Editor supports location assignments for Cyclone™, Stratix™, Stratix GX families only in this release)
- New memory compiler category in the **MegaWizard® Plug-In Manager** provides a single interface for configuring all types of memory in all device families (see Figure 1.).

Figure 1. Memory Compiler



- **Remove Assignments** dialog box (Assignments menu) allows obsolete assignments to be removed from a design easily

Synthesis

- The Synplicity Synplify software includes a new multipoint synthesis option that supports the LogicLock design flow and full DSP block inferencing for Stratix designs
- Support for new pragmas that guide synthesis results when using the Quartus II software's Integrated Synthesis option

LogicLock Block-Based Design Flow

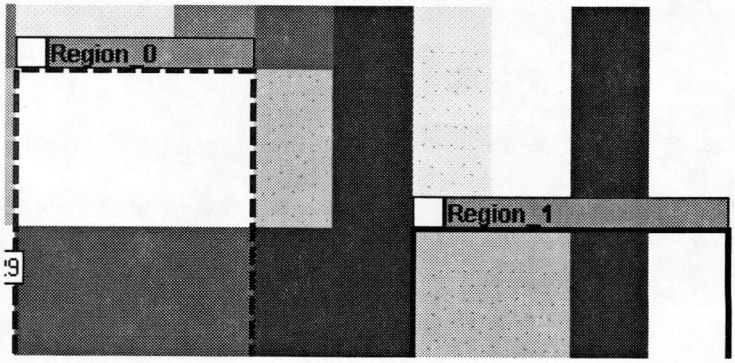
- Added ability to flip LogicLock regions horizontally for Stratix designs
- Added option to ignore LogicLock region back-annotated location contents so users can experiment with different settings without deleting assignments

Fitting & Design Optimization

- Midcompilation reporting of estimated delay from placement
- New netlist optimization option that uses fitter timing information to resynthesize and optimize a design to increase performance as much as 20%

- The **Preserve Registers** logic option assignment is available to define which registers should not be touched by the register retiming netlist optimization feature
- Timing closure floorplan improvements
  - Can now be used for all device families (not all features are available for all device families)
  - A new Routing Congestion view can be used to guide manual placement and assignment decisions, by showing congested areas highlighted in red (See Figure 2)

Figure 2. Routing Congestion View

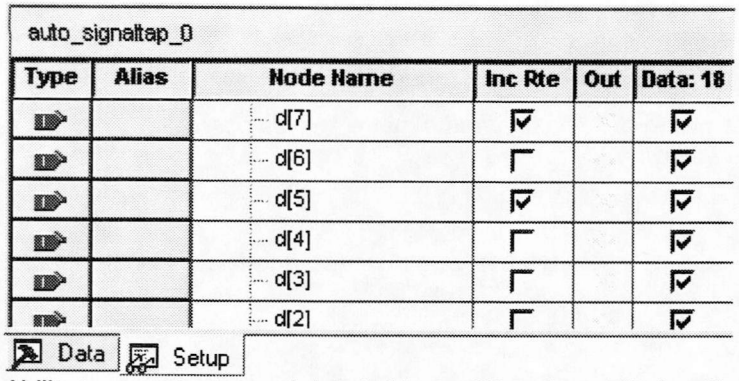


- The **Manual Logic Duplication** logic option assignment is available for Stratix, Stratix GX, and Cyclone designs
- Improved MAX® 3000A, MAX 7000B, and MAX 7000A performance by an average of 10%; Quartus II software now delivers superior performance and fitting for supported MAX devices.

Verification

- SignalTap II Embedded Logic Analyzer enhancements
  - Incremental routing capability allows users to incrementally route added or changed nodes without performing a full recompile

Figure 3. SignalTap II Includes Incremental Signal Addition/Change



  - Ability to export captured data in Vector Waveform File (**.vwf**), Table File (**.tbl**), Vector File (**.vec**), Comma-Separated Value File (**.csv**), and Verilog Value Change Dump File (**.vcd**) file formats for display and analysis in other tools
  - Resource usage estimator displays how many logic and memory resources are required for a specified SignalTap II ELA configuration
  - New status bars guide users through tasks of configuring and using the SignalTap II Embedded Logic Analyzer
- Design Assistant can now be used to identify design problems for all device families
- EDA Netlist Writer improvements
  - Automatically bring out device-wide set/reset signals as ports
  - Option to maintain design hierarchy in simulation netlists

- Generate simulation netlists with or without Stanard Delay Format (SDF) Output Files (**.sdo**) so behavioral simulation netlists can be generated at any stage of the design process
- Stratix IBIS model generation
- Synopsys PrimeTime static timing analysis support for Cyclone and Stratix GX devices

New Device Support

Table 1 shows the new device and package support in the Quartus II software version 2.2.

Table 1. New Device and Package Support in Quartus II Software Version 2.2

Family	*Device*	*Packages*
Cyclone (1)	EP1C6	F256(3)
	EP1C12	F256
Stratix (2)	EP1S20	B672(4), F672, F780
	EP1S30	F780, B956, F1020
	EP1S40	B956, F1020, F1508
	EP1S80	B956, F1508
Stratix GX (1)(5)	EP1SGX10C	F672
	EP1SGX10D	F672
	EP1SGX25C	F672
	EP1SGX25D	F672, F1020
	EP1SGX25F	F1020
	EP1SGX40D	F1020
	EP1SGX40G	F1020

Notes to Table

1. Advanced compilation & simulation support
2. Includes Programming Object File (.pof) generation
3. F = FineLine BGA® package
4. B = Ball grid array package
5. Contact your local Altera sales office for Stratix GX support

The Quartus II software supports the following device families:

- Stratix
- Stratix GX (Contact your local Altera sales office to enable Stratix GX support)
- Cyclone
- APEX™ II
- APEX 20K (including APEX 20K, APEX 20KE, and APEX 20KC)
- Excalibur™
- Mercury™
- FLEX® 10KE
- ACEX® 1K
- MAX 7000B, MAX 7000AE, MAX 3000A